a semiconductor device disposed on the planar surface of the substrate;

an encapsulant surrounding the semiconductor device wherein the encapsulant material has thermal expansion properties substantially similar to the thermal expansion properties of the substrate;

a plurality of conductive leads lengths such that the series inductance of the device package is minimized; and

said encapsulant material having a composition such that the parasitic capacitance of the device package is minimized.

Claim 14

Please amend Claim 14 as follows:

14. A surface mount semiconductor device package comprising:

a planar ceramic substrate having a first surface and an opposing second surface;

a semiconductor device disposed on the substrate first surface;

conductive pads disposed on the substrate second surface;

conductive leads coupling the semiconductor device to the conductive pads; [and]

a low dielectric constant encapsulant material encapsulating the semiconductor device and substrate first surface;

said conductive leads with lengths such that the series inductance of the device package is minimized; and

said encapsulant material having a composition such that the parasitic capacitance of the device package is minimized.

Claims 3-4 and 3-21 Objection

Claims 3-14 and 3-21 stand objected to as Claims 3 and 4 are duplicated and the numbering of Claims 5 to 21 are improper. Please retain the numbering of Claims 1 and 2 and the numbering of the first instances of Claims 3 and 4. Please renumber the second instances of Claims 3 and 4 as